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An Area Efficient High Throughput Color Demosaicking Scheme

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ABSTRACT : *A fully pipelined color demosaicking design to improve the quality of reconstructed images, a linear deviation compensation scheme was created to increase the correlation between the interpolated and neighboring pixels.*
Furthermore, immediately interpolated green color pixels are first to be used in hardware-oriented color demosaicking algorithms, which efficiently promoted the quality of the reconstructed image. A boundary detector and boundary mirror machine were added to improve the quality of pixels located in boundaries.
In addition, a hardware sharing technique was used to reduce the hardware costs of three interpolators. The VLSI architecture in this work contains only 4.97 K gate counts and the core area is 60,229 um2 synthesized by using 0.18-um CMOS process.
The operating frequency of this work is 200 MHz by consuming 4.76 mW. Compared with the previous low-complexity designs, this work has the benefits in terms of low cost, low power consumption, and high performance.

I. Introduction

Today, the majority of color cameras are equipped with a single CCD (Charge Coupled Device) sensor. The surface of such a sensor is covered by a color filter array (CFA), which consists in a mosaic of spectrally selective filters, so that each CCD element samples only one of the three-color components Red (R), Green (G) or Blue (B). The Bayer CFA is the most widely used one to provide the CFA image where each pixel is characterized by only one single color component.

To estimate the color (R, G, B) of each pixel in a true color image, one has to determine the values of the two missing color components at each pixel in the CFA image. This process is commonly referred to as CFA demosaicing, and its result as the demosaiced image. In this paper, we propose to compare the performances reached by the demosaicing methods thanks to specific quality criteria. An introduction to the demosaicing issue is given in section 2. Besides explaining why this process is required, we propose a general formalism for it. Then, two basic schemes are presented, from which are derived the main principles that should be fulfilled in demosaicing

1.1 Image Interpolation:

Image interpolation is a key aspect of digital image processing. This paper presents a novel interpolation method based on optimal recovery and adaptively determining the quadratic signal class from the local image behavior. The advantages of the new interpolation method are the ability to interpolate directly by any factor and to model properties of the data acquisition system into the algorithm itself. Through comparisons with other algorithms it is shown that the new interpolation is not only mathematically optimal with respect to the underlying image model, but visually it is very efficient at reducing jagged edges, a place where most other interpolation algorithms fail.

II. Existing System

Wide- angle cameras are widely used in surveillance and medical Imaging applications now days. Images captured by wide angle lens suffer scompressed more than the inner one. A low- cost high-speed VLSI implementation for barrel distortion correction is presented in this brief . In our simulation, the proposed circuit can achieve 200MHZ with 45K gate counts by using TSMC 0.18 mum technology. Compared with the previous distortion correction design our circuit requires less hardware cost and achieve faster working speed.

Advantage:

➢ The Circuit requires less hardware cost and achieve faster working speed.

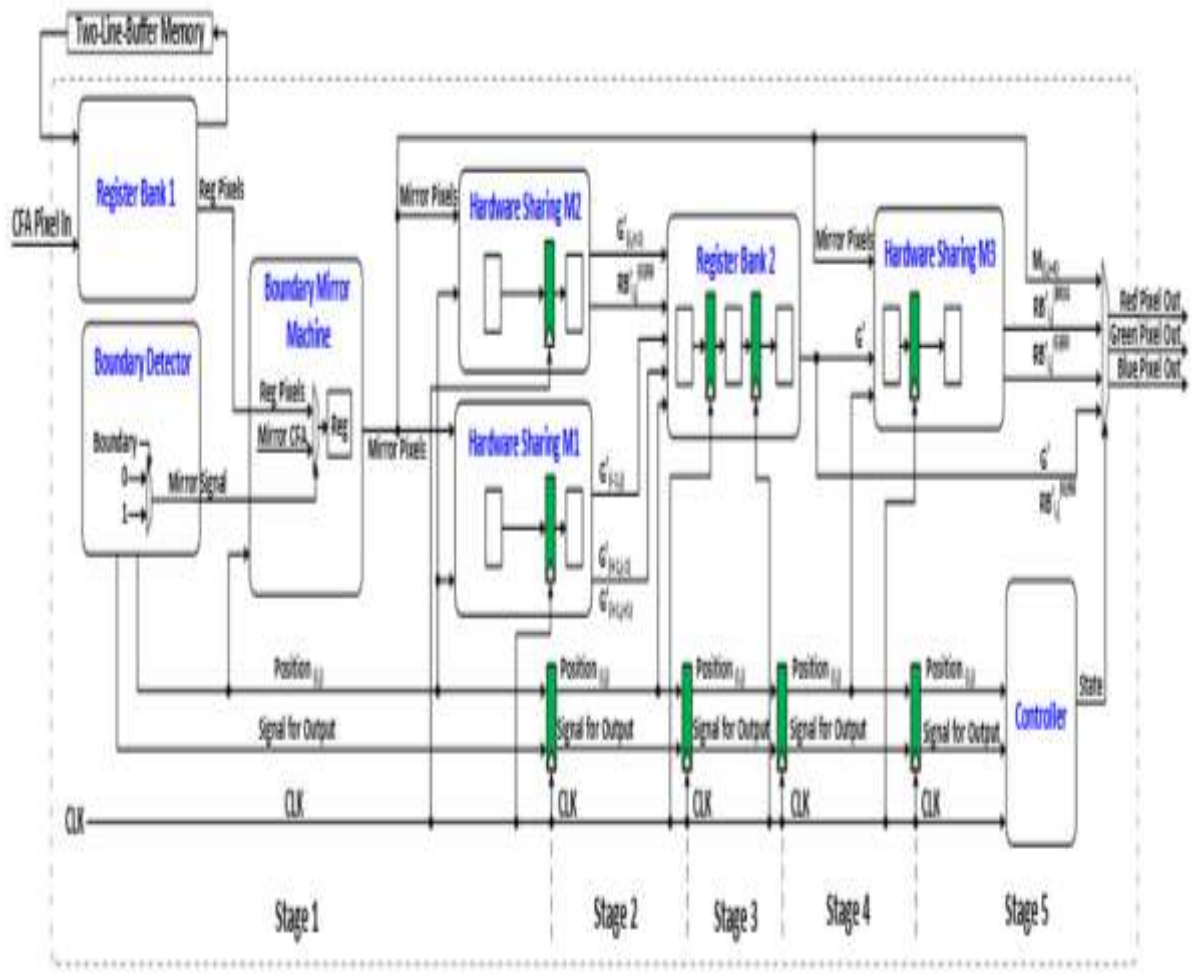
Disadvantage:

➢ Poor performance in terms of high accuracy design for real time applications in FPGA implementation.

III. Proposed System

Image interpolation is a key aspect of digital image processing. This paper presents a novel interpolation method based on optimal recovery and adaptively determining the quadratic signal class from the local image behavior. The advantages of the new interpolation method are the ability to interpolate directly by any factor and to model properties of the data acquisition system into the algorithm itself. Through comparisons with other algorithms it is shown that the new interpolation is not only mathematically optimal with respect to the underlying image model, but visually it is very efficient at reducing jagged edges, a place where most other interpolation algorithms fail.

IV. Architecture Diagram



Block Diagram of VLSI Architecture

V. Conclusion

It was proved that, the low complexity and high-performance of proposed hardware sharing and pipeline scheduling based color demosaicking VLSI design for real-time video applications. Through Linear deviation compensation, interpolated green color pixels, a boundary detector and a boundary mirror machine overall reconstruction quality of output image is increased.

FUTURE ENHANCEMENT

In this thesis a low-cost, low-memory-requirement, high-performance VLSI architecture of the color demosaicking had been proposed. To extend the hardware sharing, reconfigurable techniques can be used to reduce hardware cost. Relative to previous low-complexity, this work can achieve at least 34.5% reduction in gate counts and requires only one computational unit. To improvethe speed high speed parallel prefix adders can be used.

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